REMARKS

Claims 1-10 are all the claims pending in the application.

Applicant amends claim 1 to correct minor grammatical errors, however, these amendments are for precision of language only and do not narrow the scope of the claim.

Applicant adds new claims 11-20 to provide an alternate scope of coverage for Applicant's invention in the claims.

Applicant thanks the Examiner for acknowledging the claim for foreign priority and for placing the certified copy of the priority document in the record of the file.

The Examiner indicates that information disclosed in the IDS filed on February 16, 2000 will not be considered because it fails to comply with 37 C.F.R. § 1.98(a)(3) for not including a concise explanation of the relevance of the reference. The Examiner is incorrect because this reference is described in Applicant's specification at page 1. Thus, the concise explanation requirement is met (see MPEP 609 subsection III A(3)). Accordingly, Applicant respectfully requests the Examiner to consider this reference.

The Examiner rejects claims 1-4 and 7-10 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,486,853 to Baxter et al. and U.S. Patent 5,301,344 to Kolchinsky. The Examiner rejects claims 5 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Baxter and Kolchinsky and further in view of U.S. Patent 5,754,227 to Fukuoka. Applicant respectfully traverses these rejections. Baxter, Kolchinsky, and Fukuoka do not teach or suggest all of the features of Applicant's claimed invention.

Applicant's claimed invention defines a unique combination of features, including, *inter alia,* "executing digital image processing of an interval of active pixel" and "executing digital control processing in the condition that said first internal logic description of said field programmable gate array is: rewritten to a second internal logic description in interval of non-active pixel" (see Applicant's independent claim 1). Baxter does not disclose or suggest such a combination.

The Examiner alleges that Baxter discloses executing digital image processing in processor 66 of Figure 8 and discloses executing digital control processing in processor 70 of Figure 9. However, Figures 8 and 9 of Baxter show two separate and unrelated embodiments. Figure 8 relates to a video conferencing system (Baxter, column 7, lines 39-43), while Figure 9 relates to a camera control system for providing database management functions (Baxter, column 7, lines 46-48). Baxter does not disclose or suggest both digital control processing and digital image processing in a single embodiment. Kolchinsky does not supply this deficiency in Baxter with respect to claim 1, because Kolchinsky does not disclose or suggest digital control processing at all. Fukuoka does not address digital image processing, and therefore does not disclose this feature either.

Furthermore, claim 1 requires "executing digital image processing of an interval of active pixel in the condition that a first internal logic description is written in said field programmable gate array; [and] executing digital control processing in the condition that said first internal logic description of said field programmable gate array is rewritten to a second internal logic description". Thus, both the first and second internal logic descriptions that describe the

operation of the system during digital image processing and digital control processing are stored in the same field programmable gate array.

Baxter does not disclose or suggest this feature. In particular, in the descriptions of Figures 8 and 9, Baxter discloses that processors 66 and 70 are different types of processors that have different performance characteristics and different functions. The logic that controls the operation of the two processors is stored in the processors themselves (Baxter, column 7, lines 12-14 and lines 44-48). Even if, assuming *arguendo*, that the processor 66 executes digital image processing and processor 70 executes digital control processing as the Examiner suggests, Baxter does not disclose that the logic descriptions or programs that describe their operation are written in the same processor.

Kolchinsky does not supply the above-noted deficiencies of Baxter. In fact, Kolchinsky discloses that a single reconfigurable sequential processor would need at least two programmable gate arrays, one to act as an address generator and another to act as an arithmetic unit. (Kolchinsky, column 3, lines 23-45). Kolchinsky does not disclose that the internal logic description for the two programmable gate arrays are stored in the same programmable gate array, meaning that each programmable gate array stores its own internal logic description. Therefore, Kolchinsky does not disclose or suggest a single programmable gate array to perform both digital image processing and digital control processing as required by claim 1.

Fukuoka does not, and indeed cannot, supply the above noted deficiencies because Fukuoka does not address digital image processing or field programmable gate arrays. Since none of Baxter, Kolchinsky, or Fukuoka, considered separately or in combination, teach or

suggest the features of Applicants invention as claimed in claim 1, claim 1 is patentable over the references.

Furthermore, Applicant submits that one skilled in the art would not have been motivated to combine Baxter and Kolchinsky to achieve the Applicant's invention as claimed in claim 1. The Examiner alleges that it would have been obvious to replace the processors 66 and 70 of Baxter with the reconfigurable programmable gate arrays of Kolchinsky. Applicant respectfully disagrees. Baxter relates to video processing using specialized hardware to perform image and camera processing (Baxter, column 7, lines 1 and 2, 7 and 8, and 11-13). Kolchinsky, by contrast, relates to reconfigurable sequential processors and programmable gate arrays for use in conjunction with image data banks and general-purpose computers (Kolchinsky, Abstract and column 3, lines 15-22). Kolchinsky does not teach, disclose, or suggest that its programmable gate arrays can be used with the analog video cameras of Baxter. Furthermore, because of the specialized nature of the video hardware components discussed in Baxter, combining Baxter with Kolchinsky would require extensive redesign, experimentation, and testing in order to replace the specialized video components of Baxter with the general-purpose logic devices of Kolchinsky. There is no suggestion in either Baxter or Kolchinsky that would motivate such a combination, nor do Baxter or Kolchinsky disclose how such a combination could be accomplished.

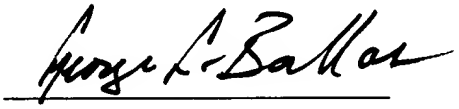
Furthermore, Fukuoka does not relate at all to digital image processing. Fukuoka relates to interfacing of a digital camera with an external input/output card for the purposes of transferring stored images and monitoring the camera's status (Fukuoka, column 1, lines 19-22 and 48-57). Because the references use incompatible components and are directed to unrelated

inventions, one of ordinary skill in the art at the time of the invention would not have been motivated to combine the references as the Examiner suggests.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: March 18, 2003

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (Amended) An image processing system provided with a field programmable gate array which is capable of altering an internal logic description, said description prescribing operation during an operating state, wherein an image processing method of said image processing system comprises~~ing the steps of~~:

executing digital image processing of an interval of active pixel in the condition that a first internal logic description is written in said field programmable gate array;

executing digital control processing in the condition that said first internal logic description of said field programmable gate array is~~:~~ rewritten to a second internal logic description in an interval of non-active pixel with the exception of said interval of active pixel; and

executing digital image processing again in the condition that said second internal description is rewritten to said first internal logic description.

Claims 11-20 are added as new claims.